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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,399	10/20/2003	Ethan Williford	2269-5864US (02-1549.00/U)	2370
24247	7590	09/08/2005	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			LOUIE, WAI SING	
			ART UNIT	PAPER NUMBER
			2814	
DATE MAILED: 09/08/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/690,399

Applicant(s)

WILLIFORD, ETHAN

Examiner

Wai-Sing Louie

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 10-29 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- “forming a transistor planar with the substrate” is not disclosed in current specification and, therefore, is a new matter.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 5, and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Yilmaz et al. (US 5,136,349).

With regard to claims 1 and 5, Yilmaz et al. disclose a closed cell transistor with built-in voltage clamp (col. 4, line 34 to col. 10, line 45 and fig. 3), comprising:

- Spaced-apart source 48a and drain 48b regions formed in the substrate 60 (fig. 3a);
- Channel region 64 defined between the source 48a and drain 48b regions (col. 5, line 51 and fig. 3a);
- A layer of gate oxide 74 formed over at least a part of the channel region 64 (col. 5, lines 19-20 and fig. 3a);
- A gate 46 formed over the layer gate oxide 74, the gate 46 further having at least one implant aperture formed (fig. 3a), the channel region 64 of the substrate 60 further including a channel internal implanted (enhancement) region 40 between the source 48a and drain 48b regions (col. 5, lines 60-65 and fig. 3a). The spaced-apart source and drain regions and the gate forming a transistor planar with the substrate (col. 3, lines 21-38).

With regard to claim 2, Yilmaz et al. disclose at least one lightly doped structure 68a located between at least one of the source 48a and drain 48b regions and the channel region 64 (fig. 3a).

With regard to claim 7, Yilmaz et al. disclose the LDD structure arranged between one of the source 48a and drain 48b regions and the channel region 64 (fig. 3a).

With regard to claims 8-9, Yilmaz et al. disclose a plurality of implant apertures arranged in a checkerboard configuration in a two dimensional array along the gate 46 (fig. 5).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yilmaz et al. (US 5,136,349).

With regard to claims 3 and 6, Yilmaz et al. disclose a channel internal implanted region 40 (fig. 3a), but do not disclose a lightly doped structure. However, Yilmaz et al. teach the region 40 becomes a diffusion source and, naturally, the substrate 60 is then subjected to a diffusing process (col. 8, lines 44-54). Thus, a lightly doped structure would be formed around the channel internal implanted region 40.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yilmaz et al. (US 5,136,349) in view of Lai et al. (US 6,649,461).

With regard to claim 4, Yilmaz et al. do not disclose the double-diffused structure 40 is implanted at a diagonal angle to the gate through the implant aperture. However, Lai et al.

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disclose an angle implant (Lai col. 8, lines 28-36 and fig. 4). Lai et al. teach the angle implant would reduce or eliminate the effects of narrow channel impurity diffusion to surrounding region of insulation (Lai col. 5, lines 48-51), which could cause the hot-carrier effect of the transistor (Lai col. 4, lines 20-35). Yilmaz et al. and Lai et al. have substantially the same environment of transistor having an oxide layer under the gate. Therefore, it would have been obvious for the one with ordinary skill in the art to modify Yilmaz's device with the teaching of Lai et al. to provide the angle implant through the gate implant aperture in order to avoid damaging the gate insulation.

### *Response to Arguments*

Applicant's arguments filed 6/9/2005 have been fully considered but they are not persuasive.

- Applicant argues the region 48a and 48b are joined outside the plane of the drawing to form an annular structure. However, the MOSFET shown in fig. 3a and 3b meets the limitations of the original presentation.

*Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (571) 272-1709. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wsl  
August 26, 2005.

LONG PHAM  
PRIMARY EXAMINER